High Resolution Digital Beamforming Receiver Using DDS-PLL Signal Generator for 5G Mobile Communication

Dong-Chan Kim, Ye-Eun Chi, Junhyeong Park, Laxmikant Minz, and Seong-Ook Park, *Senior Member, IEEE*

***Abstract*— This paper presents a signal generator and a Digital Beamforming Receiver (DBR) with high phase control resolution and high beam control resolution, respectively. The signal generator is designed based on a Direct Digital Synthesizer (DDS) and a Phase Lock Loop (PLL). In the DDS-PLL signal generator, the conventional divider in PLL is replaced with a mixer, comb generator, and a doubler to utilize high phase control resolution of DDS (14bit, 0.022°) as it is and to synchronize the DDS-PLL signal generator with the entire system. In the DBR, the output signals of the DDS-PLL signal generators are used as the second Local Oscillator (LO) signal, and the beamforming technique is implemented through the change of the phase of the second LO signals. Also, for sophisticated beamforming, all signal generator components in the DBR are synchronized for generating same and fixed frequency and phase. Finally, the DBR has the same phase control resolution as the DDS, and the phase of each chain of the DBR can be adjusted up to 0.022° (14 bit). The DBR using the DDS-PLL signal generator is designed and fabricated. The DBR consists of a 1X8 array Tapered Slot Antenna (TSA) part, a 1st and 2nd frequency conversion part, a 1X8 data acquisition and combiner part, DDS-PLL signal generator part, and a reference signal generator part. The phase control performance of the DBR was verified by measuring the phase change of the chain in the DBR according to the DDS phase change. Also, to verify the beamforming performance of the DBR with high beam control resolution, the radiation pattern of the DBR when the angle of the main lobe was 0°, 0.2°, 0.4°, 15°, and 30° was measured in the 28GHz band. At the main lobe, the gain error is within 1dB and the beam angle error is within 0.2 degrees. The simulation results are in good agreement with the measured results. A high resolution beamforming performance is achieved in the DBR using the DDS-PLL signal generator.**

***Index Terms*—Digital Beamforming, Phase Locked Loop(PLL), Direct Digital Synthesizer(DDS), millimeter-wave(mmW), 5G mobile Communication**

I. INTRODUCTION

RECENTLY, there is growing interest in 5G mobile communication-related technology. In 5G mobile communication, mm-Wave band that can secure a wide bandwidth is used for low-latency, ultra-high-speed, and super-connectivity [1]. The signal at the mm-wave band has a high path-loss, which brings great difficulty in transferring and receiving the data to a remote area. In order to overcome the difficulty, an array antenna with high gain using hundreds or thousands of arrays was introduced [2]-[5]. However, while the array antenna has a high gain, the beam width is very narrow, so it is impossible to transmit and receive communication data to objects in a wide angle range. As a solution to this problem in 5G mobile communication, beamforming technique that can adjust the angle of a beam has attracting attention [6]-[9]. Because of the sharp beam of array antenna, unlike previous mobile communication (3G/4G), beamforming technique for 5G mobile communication requires accurate and precise beam control performance in order to find targets for data transmission and reception without blind angle. Also, the beamforming technique requires the removal of unwanted directional signals in order not to affect other targets [10]-[12]. Recently, in order to implement such a beamforming technique, studies on hybrid beamforming and digital beamforming structures have been conducted [13]-[18].

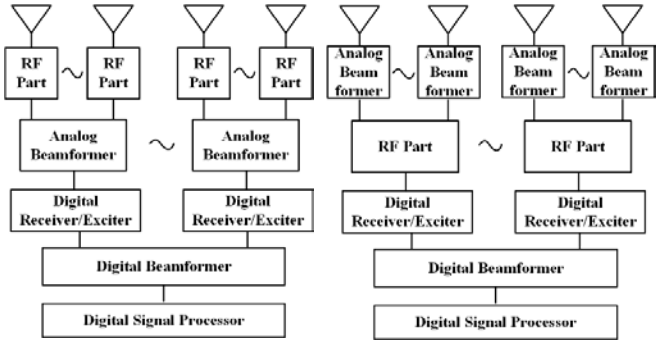


Fig. 1. The hybrid beamforming architectures

Hybrid beamforming as shown in Fig. 1 is a structure in which

This work was supported by Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government(MSIT)(No.2018-0-00733, Development of testing and verification technology for 5G mobile communications supporting eMBB, URLLC and mmTC).

This work was supported by Institute of Information & Communications Technology Planning & Evaluation(IITP) grant funded by the Korea government(MSIT)(No.2021-0-00908, K-drone detection and anti-drone integrated system development).

The authors are with the Microwave and Antenna Laboratory, School of Electrical Engineering, Korea Advanced Institute of Science and Technology(KAIST), Daejeon 34141, South Korea (e-mail: kdch5204@kaist.ac.kr, yechi@kaist.ac.kr, bdsfh0820@kaist.ac.kr, lkminz@kaist.ac.kr, soparky@kaist.ac.kr).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAP.2021.3111334, IEEE Transactions on Antennas and Propagation

analog beamformers are placed before or after the RF stage according to the desired design purpose. After changing the phase of each chain at the analog beamformer, several chains are partially bundled by an analog combiner to send signals to the baseband. This structure has the advantage of reducing the complexity of the baseband stage (ADC, DSP, etc.) and making it easier to implement. However, in the hybrid beamforming structure, a chip-based phase shifter (analog beamformer) with low phase control resolution (4~6bit) is generally used [19]-[21]. When using 4 bit phase shifter, the minimum beam adjustment angle is 5° or more, and when using 6 bit phase shifter, the beam adjustment angle is 1.14° or more. Therefore, a beam control resolution limit exists, and there are blind angles [16]. Also, since the chains are bundled together, the signals of all chains cannot be controlled and processed. In conclusion, because of the disadvantages of low beamforming resolution and low degree of freedom in signal processing, the hybrid beamforming structure alone is not suitable for use in 5G mobile communication that requires high beamforming performance.

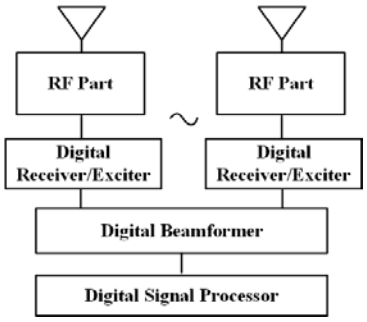


Fig. 2. The digital beamforming architectures

Unlike hybrid beamforming structure, since digital beamforming structure, Fig. 2, has a baseband stage (ADC, DSP, etc.) that collects digital signals of individual chain, the digital beamforming structure has a high degree of freedom in signal processing, and has the advantage of implementing high-resolution beamforming. However, the baseband stage of 5G mobile communication needs to collect a large number of signals from numerous chains, and these massive signals must be processed at the baseband stage. So, a high-performance baseband stage is required, and this is the limiting factor of the high performance digital beamforming implementation [11], [22-24]. A theoretically high-performance digital beamforming structure in reality has a limited beamforming resolution due to low performance baseband stage [13]. Recent researches on reducing the specifications of the baseband stage are being conducted for low complexity of the baseband stage, but reducing the specification of the baseband stage inevitably lowers the beam resolution performance of digital beamforming [25]-[28]. From this point of view, in 5G mobile communication, even when a low-performance baseband stage is used, it is necessary to achieve a high beamforming resolution of the DBF while still using the advantages of digital beamforming (high degree of freedom in signal processing). By shifting the beamforming from the digital domain, which is limited by the low performance of the baseband stage, to a high beamforming technique in the analog domain, it is possible to maintain high beamforming resolution and reduce the complexity of the baseband stage [13], [29].

In order to implement high phase control in the analog domain, several beamforming techniques using a DDS with much higher phase control resolution performance (generally 14bits or more, 0.022°) than the chip-based phase shifter have been proposed [30]-[33].

TABLE I
COMMERCIAL DDS SPECIFICATIONS

MODEL	FREQUENCY RANGE	PHASE CONTROL RESOLUTION
AD9914	< 1.75GHz	16BIT
AD9915	< 1.25GHz	16BIT
AD9959	< 0.25GHz	14BIT
AD9854	< 0.15GHz	14BIT
AD9913	< 0.125GHz	14BIT

In [30], a system capable of multi-beamforming was implemented by directly connecting only the DDS to the system. However, as shown in Table I, since the output frequency of the DDS is usually low, it is impossible to use it in the high frequency band when the DDS is directly used. Therefore, this structure has a drawback of frequency limitation and is difficult to apply to 5G mobile communication using the mm-Wave band.

In [31]-[32], beamforming technique was implemented using the DDS and PLL structures to overcome the frequency limitations of the DDS.

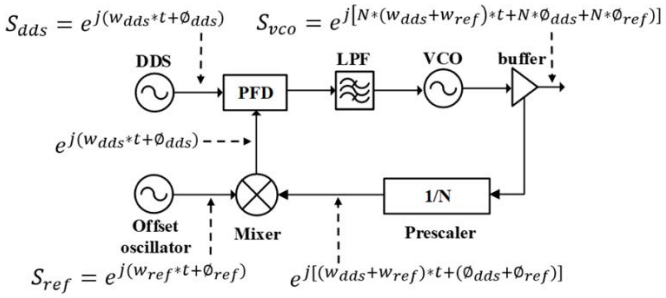


Fig. 3.The DDS-PLL block diagram in [31]

The structure used in [31] is shown in Fig. 3. In this case, the frequency of the VCO output signal is divided using a frequency divider to compare with the DDS output signal, and then down-converted again using a mixer. After the phase and frequency of the mixed signal are compared with the phase and frequency of the DDS output signal, finally, the phase of the VCO output signal is locked to the phase of the DDS. The locked VCO output signal (S_{vco}) from the phase perspective is

$$S_{vco} = e^{j[N*(w_{dds}+w_{ref})*t+N*\emptyset_{dds}+N*\emptyset_{ref})]} \quad (1)$$

where w_{dds} and $\emptyset_{dds}$ are the angular frequency and the phase of the DDS output signal, w_{ref} and $\emptyset_{ref}$ are the angular frequency and the phase of the offset oscillator output signal, N

is the value of the frequency divider. When the phase of the DDS output signal is changed as $\Delta\emptyset_{dds}$, the VCO output signal(ΔS_{vco}) is

$$\Delta S_{vco} = e^{j[N*(w_{dds}+w_{ref})*t+N*\emptyset_{dds}+N*\Delta\emptyset_{dds}+N*\emptyset_{ref})]} \quad (2)$$

where $\Delta\emptyset_{dds}$ is the phase change of the DDS output signal. In (2), the phase of the VCO output signal is changed by the product of the phase change of the DDS output signal and the frequency divider value ($N * \Delta\emptyset_{dds}$). When the frequency divider is used in the PLL structure, the phase control resolution is multiplied by the frequency divider value. Therefore, this structure has the disadvantage that it cannot use the high phase control resolution of the DDS.

In [32], it is proposed that the problem in [31] can be overcome by using an R counter. When R counter and N counter have the same value, the phase change of the VCO output signal becomes the same as the phase change of the DDS output signal. However, since the R and N counters use the same value, the PLL structure's input frequency and output frequency are the same, so it has a frequency limitation for the same reason as [30].

In [33], the beamforming technique is implemented using the DDS image signal. Specifically, in order to generate a high frequency band signal, unnecessary image frequency was removed using a band pass filter, and an image frequency signal located in the 6th nyquist zone was used. In this method, because the amplitude of the image signals is subject to sin(x)/x amplitude variation with frequency, the amplitude level of the image signals is lower than the original signal. On the other hand, the noise remains the same. Therefore, only power is lowered at the carrier frequency, so the signal characteristics (SFDR/SNR/phase noise) get worse [34]. Therefore, this method is also difficult to use for 5G mobile communication because the quality of the received signal is deteriorated by using the poor quality signal in the system.

The beamforming techniques using the DDS in [30]-[33] are suitable for specific fields, but it is difficult to implement the beamforming technique with high phase control resolution performance in a 5G mobile communication band due to the frequency constraints and the deterioration of the phase control resolution. Therefore, a new type of beamforming technique using DDS is essential for high phase control resolution in 5G mobile communication. In this paper, to implement a digital beamforming structure with the high beam control resolution at the 5G mobile communication band, a Digital Beamforming Receiver (DBR) with full advantages of the DDS is proposed.

This paper is organized as follows. In section II, the principle and architecture of the DBR are explained. It also describes a DDS-PLL signal generator without frequency constraints and deterioration of the phase control resolution. Section III discusses each part of the DBR in detail. In section IV, the measurement settings are explained, and the beamforming performance of the DBR is verified. Finally, the conclusion is in section VI.

II. Principle and Architecture of the DBR using the DDS-PLL Signal Generator

A. The principle and architecture of the DBR with high beam control resolution

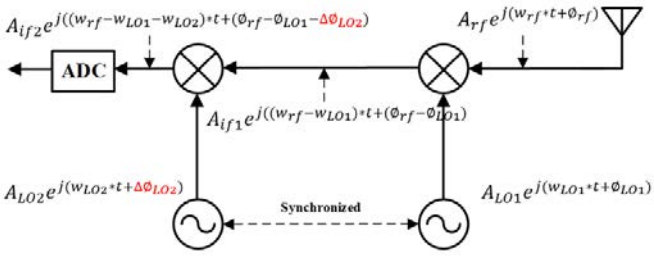


Fig. 4.The simple block-diagram of the beamforming architecture

The simple architecture of the DBR is shown in Fig. 4. In order to down-convert the Radio Frequency (RF) signal to the baseband signal, two mixers are placed and two LO signals are required. In this architecture, the principle in which digital beamforming is implemented is as follows.

In Fig. 4, the RF received signal (S_{rf}) and the 1st LO signal (S_{LO1}) are

$$S_{rf} = A_{rf}e^{j(w_{rf}*t+\emptyset_{rf})} \quad (3)$$

$$S_{LO1} = A_{LO1}e^{j(w_{LO1}*t+\emptyset_{LO1})} \quad (4)$$

where A_{rf} and A_{LO1} are the amplitude of the RF received signal and the 1st LO signal, w_{rf} and w_{LO1} are the angular frequency of the RF received signal and the 1st LO signal, $\emptyset_{rf}$ and $\emptyset_{LO1}$ are the phase of the RF received signal and the 1st LO signal. After passing through the 1st mixer, the 1st IF signal (S_{IF1}) and the 2nd LO signal (S_{LO2}) are

$$S_{IF1} = A_{IF1}e^{j[(w_{rf}-w_{LO1})*t+\emptyset_{rf}-\emptyset_{LO1}]} \quad (5)$$

$$S_{LO2} = A_{LO2}e^{j(w_{LO2}*t+\Delta\emptyset_{LO2})} \quad (6)$$

where A_{IF1} and A_{LO2} are the amplitude of the 1st IF signal and the 2nd LO signal, w_{LO2} and $\Delta\emptyset_{LO2}$ are the angular frequency and the phase of the 2nd LO signal. The last 2nd IF signal (S_{if2}) is

$$S_{if2} = A_{if2}e^{j((w_{rf}-w_{LO1}-w_{LO2})*t+(\emptyset_{rf}-\emptyset_{LO1}-\Delta\emptyset_{LO2})} \quad (7)$$

where A_{if2} is the amplitude of the 2nd IF signal. As indicated in (7), it can be confirmed that the phase of the 2nd LO signal affects the phase of the final received signal. If the phase of the 1st LO signal is fixed, it is possible to adjust the phase of the entire received signal by adjusting the phase of the 2nd LO signal. In the case of using this beamforming architecture, the phase adjustment performance of the 2nd LO signal becomes that of the entire received signal. Therefore, the phase control performance of the 2nd LO signal generator is important in this beamforming architecture.

Also, it is important to synchronize all signal generators

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAP.2021.3111334, IEEE Transactions on Antennas and Propagation

inside the beamforming architecture in order to implement sophisticated beamforming. As shown in Fig.4, three signal generator components (1st LO signal, 2nd LO signal and ADC sampling clock signal) are required per chain. Therefore, since the beamforming system is generally composed of multiple chains, a large number of signal generators exists in this beamforming architecture. When all signal generator are not synchronized with each other, two problems occur while implementing beamforming technique. The first problem in beamforming is caused by the frequency offset by several Hz between each chain. The un-synchronized oscillators could generate signal differ by several Hz depending on the external environment such as temperature, voltage current, etc [35]-[38]. and make beamforming impossible. The second problem is that it is difficult to realize accurate beamforming due to the phase difference between the signals sampled in each chain. Because if the sampling clocks between ADCs do not match, the timing at which the signals are sampled is different. As a result, a phase difference occurs between the sampled signals of each chain [39]. Therefore, in order to solve the above-mentioned problems in this beamforming architecture, it is very essential to synchronize all signal generator components.

B. The Principle and architecture of the DDS-PLL Signal Generator with High phase control resolution

To implement the aforementioned beamforming architecture with high beam control resolution, it is essential to develop the 2nd LO signal generator with high phase control resolution and a structure capable of synchronizing with the entire system. In the proposed DBR, a phase control technique with high phase control resolution is implemented using a signal generator based on a DDS and a PLL. As explained in the introduction, the frequency divider in the PLL structure adversely affects the phase control performance of the DDS-PLL signal generator. Therefore, the frequency divider is removed and instead a mixer is used for down-converting the frequency of the VCO output signal. Also, for providing the LO signal of the mixer and synchronizing the DDS-PLL signal generator to the entire system, a comb generator and a frequency multiplier are used to convert a synchronized low frequency reference signal to a synchronized high frequency LO signal of the mixer in the PLL.

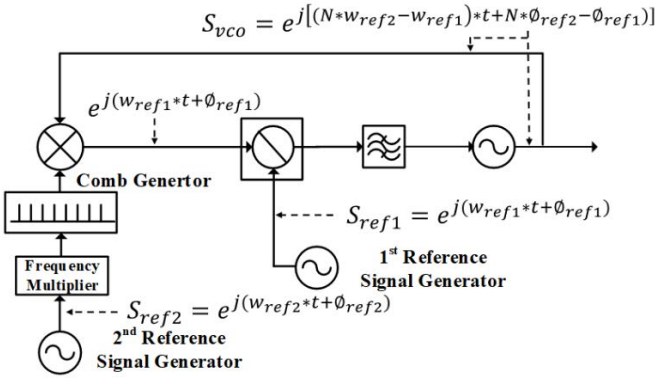


Fig. 5. The block diagram of the DDS-PLL signal generator in the proposed DBR.

Fig. 5 shows the block diagram of the DDS-PLL signal generator. In the PLL of the DDS-PLL signal generator, two reference signals are required, unlike the existing PLL structure. The first reference signal (S_{ref1}) is required for phase comparison in the Phase Frequency Detector (PFD), and the second reference signal (S_{ref2}) is used to generate the synchronized LO signals of the mixer.

In the DDS-PLL signal generator, the principle of the phase control technique is as follows. The 2nd reference signal for generating the LO signal of the mixer is

$$S_{ref2} = A_{ref2} e^{j(w_{ref2}*t+\emptyset_{ref2})} \quad (8)$$

where A_{ref2} , w_{ref2} and $\emptyset_{ref2}$ are the amplitude, angular frequency, and phase of the 2nd reference signal. The signal that passing through the frequency multiplier and comb generator is

$$S_{comb} = A_{comb} e^{j(N*w_{ref2}*t+N*\emptyset_{ref2})} \quad (9)$$

where A_{comb} is the amplitude of the signal passing through the frequency multiplier and comb generator, N is the value multiplied by the frequency multiplier value and multiplied value of the comb generator. This output signal (S_{comb}) and the VCO output signal are mixed in the mixer, and a signal (S_{mixed}) having a frequency similar to that of the 1st reference signal is generated before the PLL is locked. The signal is compared with the 1st reference signal in the PFD. The 1st reference signal and the mixed signal are

$$S_{ref1} = A_{ref1} e^{j(w_{ref1}*t+\emptyset_{ref1})} \quad (10)$$

$$S_{mixed} = A_{mixed} e^{j[(N*w_{ref2}-w_{vco})*t+N*\emptyset_{ref2}-\emptyset_{vco})]} \quad (11)$$

where A_{ref1} , w_{ref1} and $\emptyset_{ref1}$ are the amplitude, angular frequency, and phase of the 1st reference signal, w_{vco} and $\emptyset_{vco}$ are the angular frequency and phase of the VCO output signal and A_{mixed} is the amplitude of the mixed signal. Finally, when the VCO output signal is locked to the 1st reference signal, the phase and frequency of the output signal of the mixer become equal to the phase and frequency of the 1st reference signal.

$$S_{mixed} = S_{ref1} \quad (12)$$

Finally, the VCO output signal is

$$S_{vco} = A_{vco} e^{j[(N*w_{ref2}-w_{ref1})*t+N*\emptyset_{ref2}-\emptyset_{ref1})]} \quad (13)$$

where A_{vco} is the amplitude of the VCO output signal. When the phase of the 1st reference signal is changed, the 1st reference signal is

$$S_{ref1} = A_{ref1} e^{j(w_{ref1}*t+\emptyset_{ref1}+\Delta\emptyset_{ref1})} \quad (14)$$

where $\Delta\emptyset_{ref1}$ is the phase change of the 1st reference signal. When the phase of the 1st reference signal is changed, the VCO

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAP.2021.3111334, IEEE Transactions on Antennas and Propagation

output signal is

$$S_{vco} = A_{vco} e^{j[(N*w_{ref2} - w_{ref1})*t + N*\emptyset_{ref2} - \emptyset_{ref1} - \Delta\emptyset_{ref1}]} \quad (15)$$

As shown in (15), it can be confirmed mathematically that the phase change of the VCO output is same as the phase change of the 1st reference signal. Therefore, when the 1st reference signal is provided by a signal generator capable of phase adjustment with high phase control resolution and the 2nd reference signal is provided by a signal generator synchronized to the entire system, the VCO output signal can be accurately and finely adjusted.

III. Design of the DBR

A. System Architecture

The full architecture of the proposed DBR is shown in Fig. 6. The proposed DBR is designed using the principle and architecture of the digital beamforming technique and the DDS-PLL signal generator described in Section II. The DBR has 8 chains, and each chain consists of the TSA array part, 1st & 2nd frequency conversion part, and data acquisition & combiner part. And, as a key part of the DBR, there are the DDS-PLL signal generator part and the reference signal generator part.

In order to synchronize the entire system, the reference signal generator part generates reference signals by using a frequency doubler and a divider from the output signal of a 100MHz oscillator. The DDS-PLL signal generator part consists of DDS and PLL, and the output signals are controlled by the DDS with high phase control resolution and are synchronized by the reference signals from the reference signal generator part. The 1X8 Array TSA is composed of 8 element antennas and serves to receive RF signals. In the 1X8 1st Frequency conversion part, consist of the Low Noise Amplifiers (LNAs), filters, mixer, and frequency doublers, the signal received through the 1x8 array TSA is amplified by LNA, and then is mixed with the 1st LO signal synchronized by the signal of the reference signal generator part. After passing the 1X8 1st Frequency conversion part, the RF signal is down-converted into the 1st IF signal. In the 1X8 2nd frequency conversion part, consist of the attenuators, filters, amplifiers, and mixers, unnecessary signals included in the 1st IF signal are removed by using filters and attenuators, and the 1st IF signal is down-converted to the 2nd IF signal using the 2nd LO signal from the PLL-DDS signal generator part. In this down-conversion process, beamforming is implemented by controlling the phase of the 2nd LO signal with high phase control resolution. In the 1X8 Data Acquisition & Combiner part, the 2nd IF signal is sampled as a digital signal through an ADC in the SDR, and unnecessary signals are removed through a digital band pass filter (BPF). Finally, the signals received from each chain are combined by the digital combiner.

For each of the parts described above, all signal generator components are synchronized with each other by using the reference signal generator part, and the phase of the entire received signals of the DBR is controlled by adjusting the DDS-PLL signal generator part. Finally, the proposed DBR can have accurate and precise beamforming performance with high beam control resolution. Details of each part are described below.

B. The DDS-PLL Signal Generator Part

The DDS-PLL signal generator part architecture is shown in Fig. 7. The DDS-PLL signal generator part is composed of 8 chains to apply for 8 chains of the DBR. Two DDS (AD9959) are used and synchronized with each other by the reference signals generated from the reference signal generator part. Synchronized DDS output signals are used as the 1st reference signals in Fig. 5, and the reference signals generated in the reference signal generator part of the DBR are used as the 2nd reference signals in Fig. 5. The frequency and output power of the DDS-PLL signal generator are 3.5GHz and about 9dBm as shown in Fig. 8. Comparing with the specifications of the 2nd frequency conversion part in Table V, it can be confirmed that

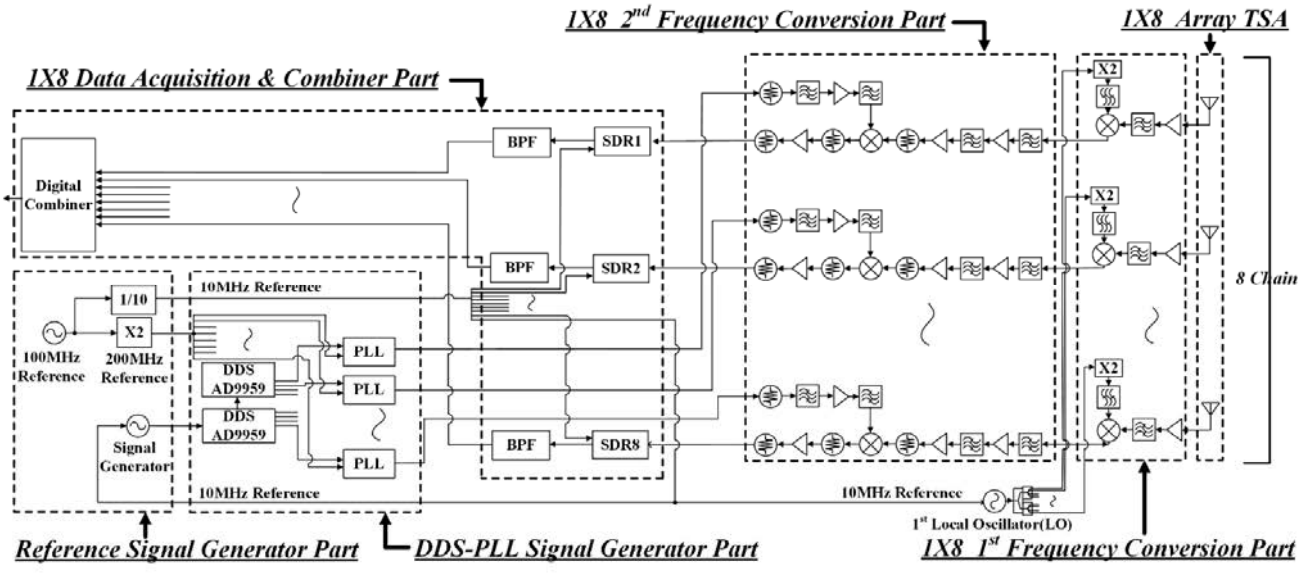


Fig. 6. The full architecture of the DBR using DDS-PLL signal generator.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAP.2021.3111334, IEEE Transactions on Antennas and Propagation

the output power of the DDS-PLL signal generator part is suitable for use in the 2nd frequency conversion part. Also, the measured phase noise of the DDS-PLL signal generator from 10 kHz to 10 MHz is shown in Fig. 9. The loop filter of the PLL has a loop bandwidth about of 20kHz and is designed for reliable spur removal by considering the specs of its components (VCO, charge pump, etc.) in the DDS-PLL signal generator. The phase noise values at the main frequencies are listed in Table II. Comparing the phase noise of the PLLs of [40] and [41] in similar frequency bands, it can be confirmed that the DDS-PLL signal generator has good phase noise characteristics.

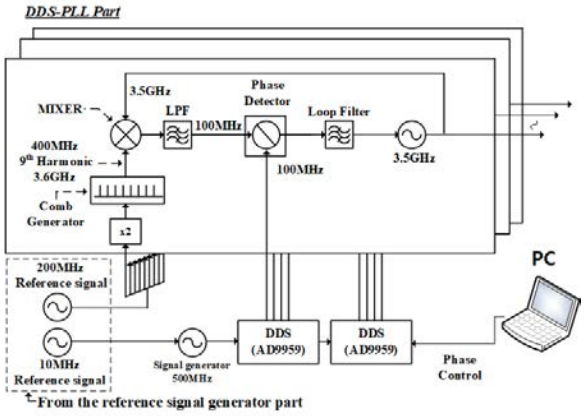


Fig. 7. The block diagram of the DDS-PLL signal generator.

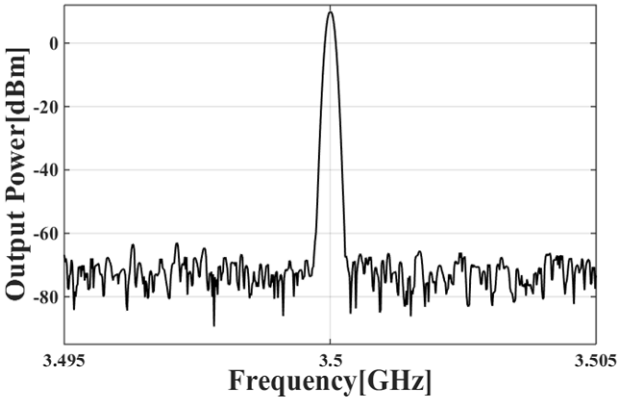


Fig. 8. The measured output power of the DDS-PLL signal generator.

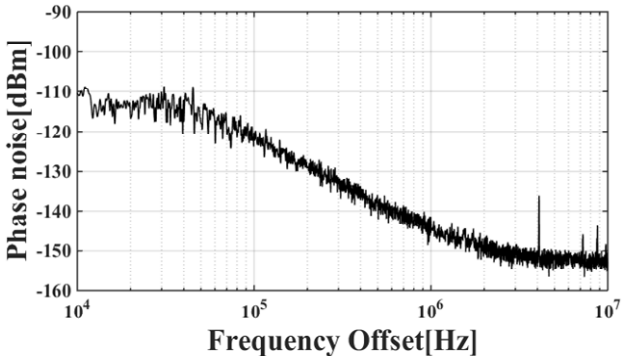


Fig. 9. The measured phase noise of the DDS-PLL signal generator.

TABLE II
THE PHASE NOISE OF THE DDS-PLL OUTPUT

PHASE NOISE	
FREQUENCY	PHASE NOISE[DBC/HZ]
10KHZ	-110.5
100KHZ	-122.3
1MHZ	-142.4
10MHZ	-152.6

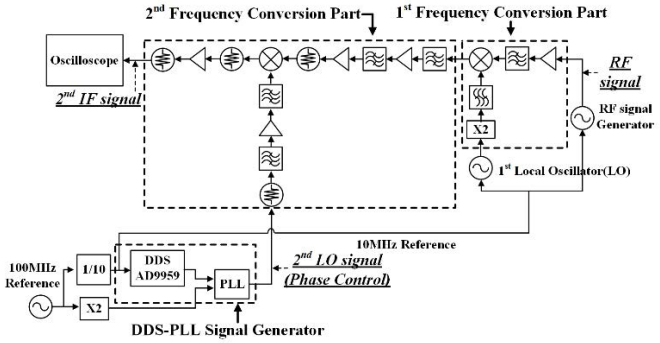


Fig. 10. 2nd IF signal measurement setup

In order to confirm the phase control performance of the DDS-PLL signal generator, the phase change of the 2nd IF signal of the DBR with the phase change of the DDS output signal is measured. The reason for measuring the phase of the 2nd IF signal without measuring the phase of the output signal of the DDS-PLL signal generator is that it is difficult to measure the phase of a signal in the frequency band above 1GHz unless expensive measurement equipment is used. Unlike the output signal of the DDS-PLL signal generator, the 2nd IF signal has a frequency of 1 GHz or less, and as described in section II, the phase of the 2nd IF signal is changed in the same as the phase change of the DDS output signal. Therefore, by measuring the phase change of the 2nd IF signal according to the phase change of the DDS output signal, the overall phase control performance of the DDS-PLL signal generator and the DBR can be verified. In Fig. 10, the 2nd IF phase measurement setup consists of an RF signal generator that generates an RF signal within the system dynamic range and bandwidth, a chain of DBR, and an oscilloscope that measures the 2nd IF phase. The RF signal generated from the RF signal generator passes through one chain of DBR, and the phase change of the 2nd IF signal according to the phase change of the DDS output signals is measured by the oscilloscope.

TABLE III
DDS PHASE CHANGE & MEASURED PHASE CHANGE [UNIT : DEGREE]

DDS PHASE CHANGE	MEASURED 2ND IF PHASE CHANGE
1.0107	1
2.0214	2
3.0102	3
4.0210	4
5.0010	5
6.0205	6
7.0092	7
8.0200	8
9.0087	9
10.0195	10

Table III show the measurement results of the phase change of the 2nd IF signal with the phase change of the DDS output signal. Since the measurable phase resolution of the owned oscilloscope is 0.5° or more, the measurement is conducted with phase changes at 1° interval. Through the measurement results, it can be confirmed that the phase change of the 2nd IF output signal is almost the same as the phase change of the DDS output signal. If precise measuring equipment is used, it would be possible to verify high phase control performance of the DDS-PLL signal generator part of about 0.02°.

C. Reference Signal Generator Part

The reference signal generator part serves to synchronize all signal generator components in the DBR. As shown in Fig. 6, the base signal of the reference signal generator part is generated in the 100MHz source, and ten 10MHz signals and eight 200MHz signals are generated from the base signal. The signals are used as reference signals of signal generator components. The frequency of the base 100MHz signal is firstly divided by 1/10 to generate a 10MHz reference signal. After the 10MHz reference signal passes through the 1:10 divider, the 10MHz reference signals are distributed to each part that needs a reference signal. The 1:10 divider not only serves as a signal distribution, but also serves to control the power of the signals to the power required for each part. The distributed 10MHz signals are used as reference signals of signal generators generating a reference signal of the DDS and the 1st LO signal of the 1st frequency conversion part. Also, the 10MHz signals are used as each ADC sampling clock. Secondly, the base 100MHz signal passes through the frequency doubler and the 1:8 divider and is converted into eight 200MHz signals. Like the 1:10 divider, the 1:8 divider not only serves as a signal distribution, but also serves to control the power of the signals to the power required for each part. These eight 200MHz signals are used as reference signals for generating synchronized LO signals inside the PLL of the DDS-PLL signal generator part. In this way, all clock signals and reference signals are synchronized to the base 100MHz signal, and the aforementioned problems in Part II can be solved.

D. 1X8 1st & 2nd Frequency Conversion Part

In the DBR, the 1st frequency conversion part consists of 8 Low Noise Blocks (LNBs). The LNBs perform the role of down-converting the RF signal to the 1st IF signal and amplifying the RF signal while reducing noise. Since the phase and frequency of the 1st LO signals affect the entire system in beamforming, the synchronized signals should be used as the LO signals. In order to generate the LO signals having same and fixed phase and frequency, one signal synchronized by the reference signal generator part is divided into 8 signals using a 1:8 divider, and the 8 signals are used as the LO signals. The specifications for the LNB used are given in Table IV and the LNB has adequate performance at 28GHz band (5G mobile communication band).

The 2nd frequency conversion part down-converts the 1st IF signal to the 2nd IF signal and serves to change the phase of the received signal in each chain of the DBR. As the LO signals of the 2nd frequency conversion part, the output signals of the DDS-PLL signal generator part capable of phase shift are used. The 2nd frequency conversion part was designed and fabricated considering the performance of the DDS-PLL signal generator part and the 1st frequency conversion part. To confirm the performance of the fabricated 2nd frequency conversion part, major parameter measurements were performed. The measurement results are shown in Table V and it can be confirmed that when the 2nd frequency conversion part is connected with the 1st frequency conversion part and the DDS-PLL signal generator, the 2nd frequency conversion part has an appropriate frequency band and suitable LO signal required power.

TABLE IV
THE SPECIFICATION OF THE 1ST CONVERSION PART

THE SPECIFICATION	
MANUFACTURER	ANALOG DEVICES
MODEL NUMBER	HMC1065LP4E
RADIO FREQUENCY (GHz)	27 ~ 34
LOCAL OSCILLATOR FREQUENCY (GHz)	11.5 ~ 19
LOCAL OSCILLATOR POWER(DBM)	-4 ~ 4
IF FREQUENCY(GHZ)	DC ~ 4
FLATNESS (dB)	< 1
CONVERSION GAIN (dB)	12

TABLE V
THE SPECIFICATION OF 2ND CONVERSION PART

THE SPECIFICATION	
RADIO FREQUENCY (GHz)	2.536 ~ 3.374
LOCAL OSCILLATOR FREQUENCY (GHz)	3.5
LOCAL OSCILLATOR POWER(DBM)	>7
IF FREQUENCY(GHZ)	0.126 ~ 0.964
FLATNESS (dB)	< 1
CONVERSION GAIN (dB)	17

E. 1X8 Data Acquisition & Combiner Part

TABLE VI
THE SPECIFICATION OF THE ADC

THE SPECIFICATION	
MODEL	MAX5864
RESOLUTION (BIT)	8
SAMPLE RATES (MSPS)	1~20
SNR (dB)	48.6
SINAD (dB)	48.5
SFDR (dBc)	69

TABLE VII
THE SPECIFICATION OF THE SDR

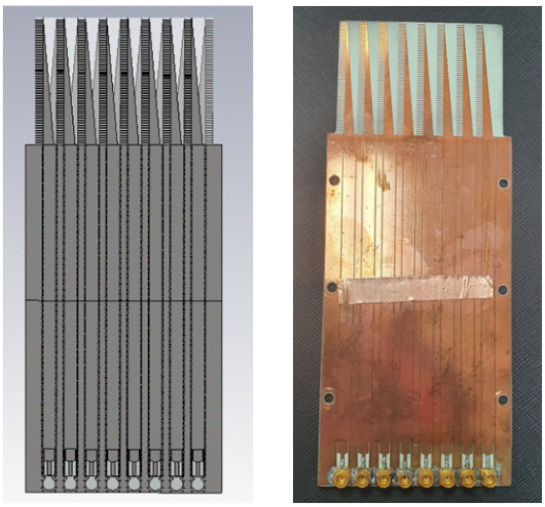
THE SPECIFICATION	
RECEIVED FREQUENCY (GHz)	0.001 ~ 6
GAIN OF VGA IN IF (dB)	0 ~ 40
GAIN OF VGA IN BASE BAND(dB)	0 ~ 62
SAMPLING RATE (MHz)	< 20
FLATNESS (dB)	<1
MAXIMUM DYNAMIC RANGE (dB)	75

The data acquisition and combination proceed in the Software Defined Radios (SDRs). The SDR is composed of Variable Gain Amplifiers (VGAs), IQ demodulator, and ADC. The ADC specifications used are listed in Table VI. Considering the dynamic performance of the ADC (SNR, SINAD, SFDR, etc.) that can measure the beamforming performance of the proposed DBR, the ADC (MAX5864) was selected and used. The measured specification of the SDR is listed in Table VII. Using the reference signal generator part of the DBR, the signal

generator components inside the SDRs such as the sampling clocks and the signal generators are synchronized to the DBR. The signals received on each chain are sampled in the ADCs, and the sampled signals are combined by the digital combiner after passing the digital filter.

F. The 1X8 Array TSA Part

Fig. 11-(a) shows the design of the 1X8 array TSA used in the antenna part of the DBR. The 1X8 array TSA is designed with the same specifications except for the coupler and divider on the TSA antenna in [13]. The 1X8 array TSA is composed of single antennas, Substrate Integrated Waveguide (SIW) lines, and microstrip to SMP transitions. The fabricated 1X8 array TSA showed in Fig. 11-(b) is used as the antenna part in the DBR. Fig. 12 shows the measured and simulated return loss of the element antenna of the 1X8 array TSA. The return losses are -10dB or less in the 28GHz band, and the measured results are in good agreement with the simulated results. The simulation results of the radiation pattern in which the angle of the main lobe is 0°, 15°, and 30° are shown in Fig. 13, which confirms that the main lobe is adjusted to the desired angle.



(a) (b)

Fig. 11. (a) Structure of the 1X8 array TSA in the simulation and (b) Fabricated the 1X8 array TSA.

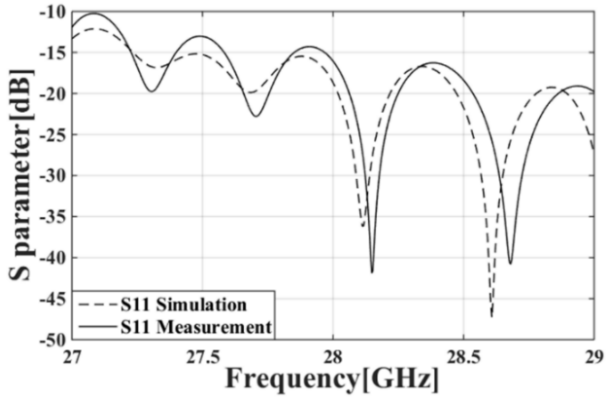


Fig. 12. The simulated and measured return loss of the element Antennas-parameter

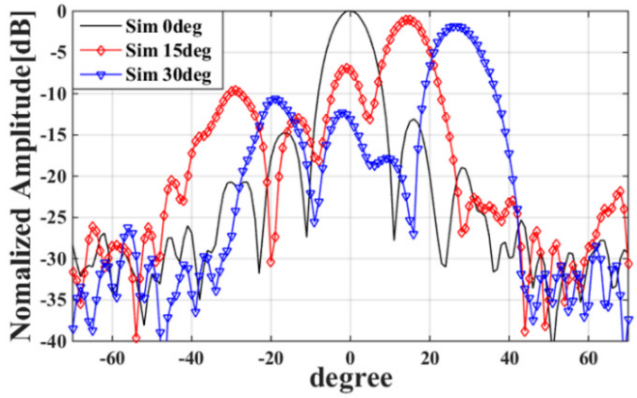
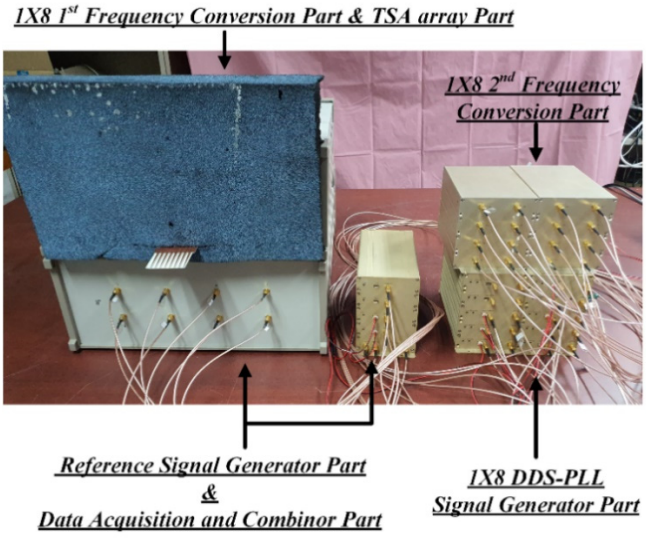
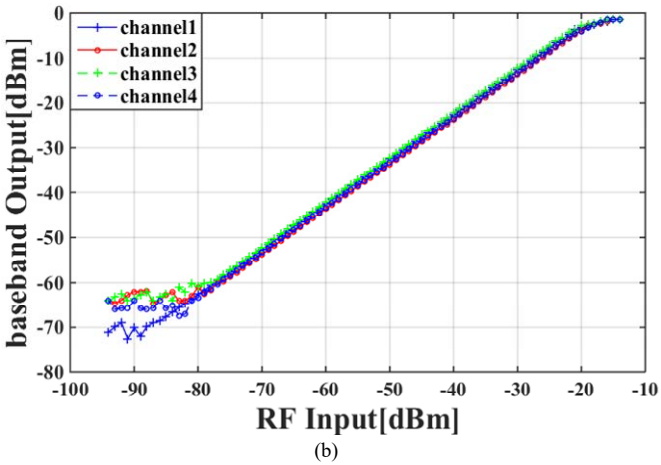


Fig. 13. The Simulation radiation pattern result of the 1X8 TSA antenna.

G. The overall performance of the DBR



(a)



(b)

Fig. 14. (a) The fabricated DBR and (b) The measured dynamic range result of the DBR.

Fig. 14-(a) shows the fabricated DBR. The phase control performance of the DBR has already been verified in the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAP.2021.3111334, IEEE Transactions on Antennas and Propagation

description of the DDS-PLL signal generator part. Additionally, In order to implement a sophisticated beamforming technique in beamforming system, securing the linearity of each chain is essential [42]. In order to verify the linearity of each chain of the DBR, the dynamic range was measured, and the measurement results of the dynamic range of each chain are shown in Fig. 14-(b). As shown in the measurement results, it can be seen that the linearity of each chain is secured within the dynamic range of the DBR.

The total specifications of the DBR are listed in Table VIII. The operation frequency band of the DBR includes a 5G mobile communication band, and the DBR has 14 bit phase control resolution. Based on the phase control resolution, the theoretical minimum beam control resolution of the DBR is calculated, which is 0.01°.

TABLE VIII
TOTAL SPECIFICATION OF THE DBR

THE SPECIFICATION	
RADIO FREQUENCY (GHz)	27 ~ 34
1ST LOCAL OSCILLATOR FREQUENCY (GHz)	11.5~ 19
1ST LOCAL OSCILLATOR POWER(DBM)	-4 ~ 4
1ST IF FREQUENCY (GHz)	2.536 ~ 3.374
2ND LOCAL OSCILLATOR FREQUENCY (GHz)	3.5
2ND LOCAL OSCILLATOR POWER(DBM)	>7
2ND IF FREQUENCY(GHz)	0.126 ~ 0.964
PHASE CONTROL RESOLUTION (BIT)	14
THEORETICAL BEAM CONTROL RESOLUTION (°)	0.01
FLATNESS (dB)	< 1.5
CONVERSION GAIN (dB)	16 ~ 17

IV. THE BEAMFORMING PERFORMANCE MEASUREMENT RESULT OF THE DBR

A. The Experiment Setting

In order to verify the high beamforming performance of the proposed DBR using the DDS-PLL signal generator, the radiation pattern was measured in the anechoic chamber as shown in Fig. 15. As a transmitting antenna, the 28GHz band horn type probe antenna shown in Fig. 16-(a) was used, and has a gain of about 10dB at 28GHz as shown in Fig. 16-(b). The transmitted signal is generated using the signal generator equipment. The signal generator equipment is also synchronized using the 10MHz reference signal from the reference signal generation part.

The frequencies used for the measurement are as follows. The RF frequency, 1st LO frequency, and 2nd LO frequency are 28GHz, 14GHz, and 3.5GHz, respectively. The 1st IF frequency and 2nd IF frequency are 3GHz and 0.5GHz, respectively. In order to verify the overall beamforming performance of the DBR, the radiation patterns with the main lobe at 0°, 15°, and 30° are measured by rotating the motor by 1 degree intervals. Also, in order to measure high beam control resolution performance, the radiation patterns are measured when the main lobe angle are 0°, 0.2°, and 0.4° degrees. The reason for setting the angle in 0.2 degree intervals is that the 0.2° interval is the minimum control angle resolution of the motor used to rotate the DBR. Table IX shows the weighting factors applied for each main lobe angle.

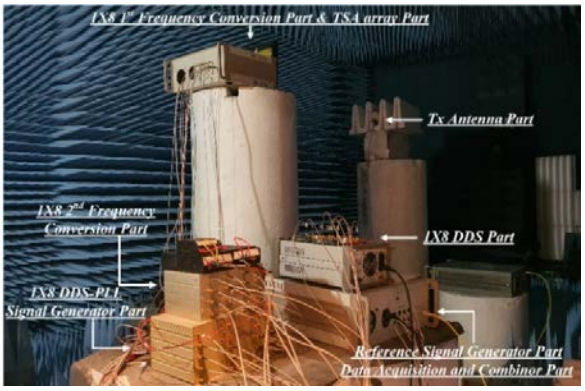
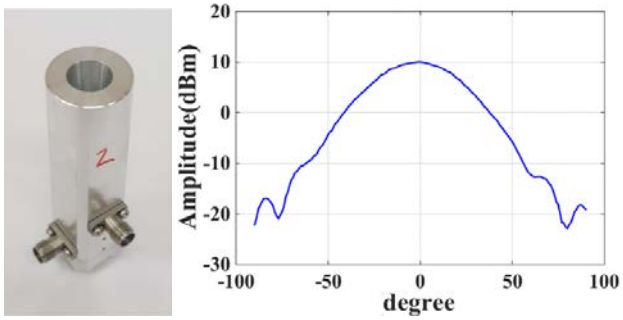


Fig. 15. The experiment setting in the anechoic chamber.



(a) (b)

Fig. 16. (a) The fabricated transmit antenna and (b) The measurement result of the transmit antenna.

TABLE IX
WEIGHTING FACTOR (UNIT : DEGREE)

BEAM ANGLE	WEIGHTING FACTOR							
	$\emptyset_1$	$\emptyset_2$	$\emptyset_3$	$\emptyset_4$	$\emptyset_5$	$\emptyset_6$	$\emptyset_7$	$\emptyset_8$
0	0	0	0	0	0	0	0	0
0.2	-2.6	-1.9	-1.1	-0.4	0.4	1.1	1.9	2.6
0.4	-5.2	-3.7	-2.2	-0.7	0.7	2.2	3.7	5.2
15	-193.9	-138.5	-83.1	-27.7	27.7	83.1	138.5	193.9
30	-374.6	-267.6	-160.5	-53.5	53.5	160.5	267.6	374.6

B. The Calibration

After turning on the power of the DBR, the phase and amplitude of each chain change as the temperature rises [43]-[46]. When the temperature of the DBR saturates, the changes of the phase and amplitude also saturate. After the saturation of the phase and amplitude changes in the DBR, external calibration is performed to calibrate these changes. The transmit antenna is placed in the far-field region and emits a signal. The emitted signal enters each chain with the same phase and magnitude. The phase and magnitude of the signal are measured after passing through each chain at the 2nd IF stage. The phase differences between each chain are calibrated by changing the phase of the output signal of the DDS-PLL signal generator, and the amplitude difference between each chain is calibrated using the VGAs of the SDR.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAP.2021.3111334, IEEE Transactions on Antennas and Propagation

C. *The Measurement Result*

The radiation pattern measurement results are shown in Fig. 17. Comparing the measured radiation pattern with beamforming angles of 0°, 15°, and 30° with the simulated radiation pattern, the measured main lobe angles are almost same as the main lobe angles of the simulation results. In case of the gain error, the gain errors in the main lobe (the angle : ±5° from the central angle) are within 1dB, whereas errors in side lobe are comparatively large. These errors mainly occur because of the difference in the simulation environment and the actual measurement environment. In the simulation, it is the result of assuming free space, but in the actual measurement, the measurement errors occurred due to the structures supporting the antenna/system and the manufacturing process error of the antenna. Fig. 18 shows the radiation pattern results of measuring the beam adjustment angle at 0.2° intervals to demonstrate the high beam control performance of the DBR. The errors of each main lobe angle between the simulated and measured result are within 0.2°. It can be confirmed that the measurement results are in good agreement with the simulation results and that the beam is precisely and finely adjusted. If a motor with an angle adjustment resolution of less than 0.2° is used, higher beamforming performance than the one currently measured can be confirmed.

V. CONCLUSION

In order to implement a precise and fine beamforming technique for the 5G mobile communication, various beamforming structure has been studied. However, there are still many difficulties in implementing precise beamforming technique. In this paper, the DBR with high beam control resolution in the 5G mobile communication band is proposed. In the DBR, the phase of each chain is controlled using the DDS-PLL signal generator part with 14 bits (0.022°) phase control resolution. And, based on the phase control resolution, the DBR theoretically has beamforming performance with a minimum beam control resolution of about 0.01°. In order to prove the beamforming performance of the DBR, the DBR was fabricated, and the radiation patterns of the DBR were measured when beam angle is at 0°, 0.2°, 0.4°, 15°, and 30°. The error of the angle of the main lobe is within 0.2°, and the gain error of the main lobe is within 1dB, which confirms that the measurement results matched well with the simulation results. Therefore, the DBR has a good candidate structure for 5G mobile communication that requires high beamforming performance. Additionally, according to the technology flow that the 5G mobile communication system is manufactured based on SOC (System on Chip), the proposed DBR needs to consider implementation based on SOC to be used in 5G mobile communication. When implementing the DBR based on SOC, because there are many oscillators and various active components in the proposed DBR, high isolation performance between components is required so that the output signals of oscillators and signals (desired and unwanted signals) generated by various active components do not affect other components. Therefore, considering that research on SOC at the component level and system level is also actively progressing in the 5G mobile communication band and chip manufacturing technology is rapidly developing [47]-[53], the DBR can be sufficiently implemented if higher isolation between components is secured than the existing SOC design.

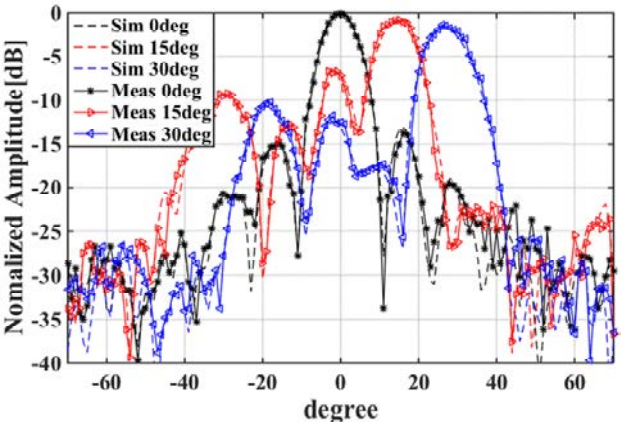


Fig. 17. The measured and simulated beamforming result of the proposed DBR at 0°, 15°, 30°.

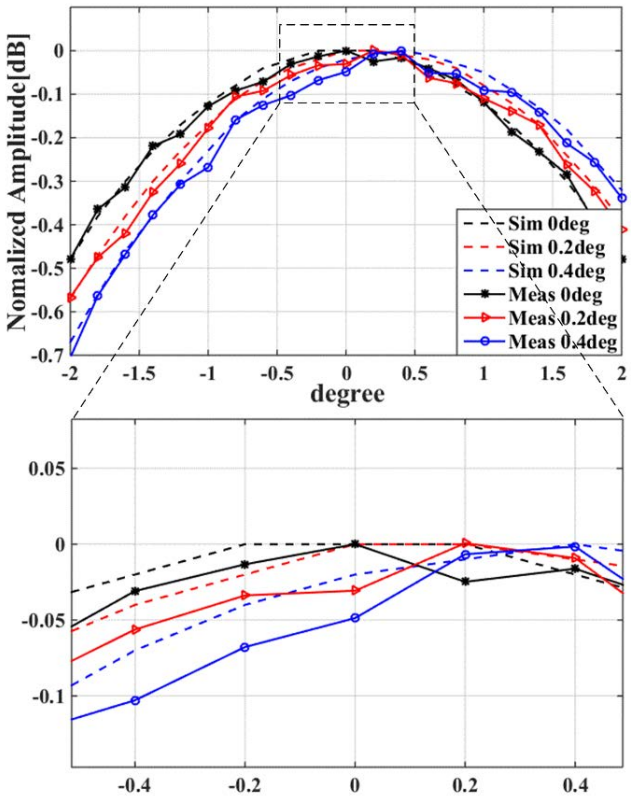


Fig. 18. The measured and simulated beamforming result of the proposed DBR at 0°, 0.2°, 0.4°.

REFERENCES

[1] M. Shafi et al., "5G: A tutorial overview of standards, trials, challenges, deployment, and practice," *IEEE J. Sel. Areas Commun*., vol. 35, no. 6, pp. 1201–1221, Jun. 2017.

[2] J. G. Andrews et al., ''What will 5G be?,'' *IEEE J. Sel. Areas Commun*., vol. 32, no. 6, pp. 1065–1082, Jun. 2014.

[3] N. Ghassemi, K.Wu, S. Claude, X. Zhang, and J. Bornemann, "Low-cost and high-efficient w-band substrate integrated waveguide antenna array made of printed circuit board process," *IEEE Trans. Antennas Propag* vol. 60, no. 3, pp. 1648–1653, Mar. 2012.

[4] Y. Yu, W. Hong, Z. H. Jiang, and H. Zhang, "E-band low-profile, wideband 45° linearly polarized slot-loaded patch and its array for millimeterwave communications," *IEEE Trans. Antennas Propag.*, vol. 66, no. 8, pp. 4364–4369, Aug. 2018.

[5] Y. Yu, W. Hong, H. Zhang, J. Xu, and Z. H. Jiang, "Optimization and implementation of SIW slot array for both medium- and long-range 77 GHz automotive radar application," *IEEE Trans. Antennas Propag.*, vol. 66, no. 7, pp. 3769–3774, Jul. 2018.

[6] Y. Li, J. Wang, and K.-M. Luk, ''Millimeter-wave multibeam aperturecoupled magnetoelectric dipole array with planar substrate integrated beamforming network for 5G applications,'' *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6422–6431, Dec. 2017.

[7] O. Jo, J.-J. Kim, J. Yoon, D. Choi, and W. Hong, ''Exploitation of dual-polarization diversity for 5G millimeter-wave MIMO beamforming systems,'' *IEEE Trans. Antennas Propag*., vol. 65, no. 12, pp. 6646–6655, Dec. 2017.

[8] S. Han, C.-L. I, Z. Xu, and C. Rowell, "Large-scale antenna systems with hybrid analog and digital beamforming for millimeter wave 5G," *IEEE Commun. Mag*., vol. 53, no. 1, pp. 186–194, Jan. 2015.

[9] J. Lota, S. Sun, T. S. Rappaport, and A. Demosthenous, "5G uniform linear arrays with beamforming and spatial multiplexing at 28, 37, 64, and 71 GHz for outdoor urban communication: A two-level approach," *IEEE Trans. Veh. Technol*., vol. 66, no. 11, pp. 9972–9985, Nov. 2017.

[10] R. Zhang, J. Zhou, J. Lan, B. Yang, and Z. Yu, '''A high-precision hybrid analog and digital beamforming transceiver system for 5G millimeter-wave communication,,'' *IEEE Access*, vol. 7, pp. 83012–83023, 2019.

[11] Y. Liu, X. Shi, S. He, and Z. Shi, "Prospective positioning architecture and technologies in 5G networks," *IEEE Netw*., vol. 31, no. 6, pp. 115–121, Nov./Dec. 2017.

[12] S. A. Busari, K. M. S. Huq, S. Mumtaz, L. Dai, and J. Rodriguez, "Millimeter-Wave massive MIMO communication for future wireless systems: A survey," *IEEE Commun. Surveys Tuts*., vol. 20, no. 2, pp. 836–869, 2nd Quart., 2018.

[13] D. Kim, S. Park, T. Kim, L. Minz, and S. Park, "Fully Digital Beamforming Receiver With a Real-Time Calibration for 5G Mobile Communication," *IEEE Transactions on Antennas and Propagation*, vol. 67, no. 6, pp. 3809–3819, June 2019.

[14] R. Miura et al., "Beamforming Experiment with a DBF Multibeam Antenna in a Mobile Satellite Environment*," IEEE Trans. Antennas Prop*., vol. AP-45, no. 4, Apr. 1997, pp. 707-14

[15] J. S. Herd and M. D. Conwy, "The evolution to modern phased array architectures," *Proc. IEEE*, vol. 104, no. 3, pp. 519–529, Mar. 2016

[16] B. Sadhu et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017

[17] T. E. Bogale, L. B. Le, A. Haghighat, and L. Vandendorpe, "On the number of RF chains and phase shifters, and scheduling design with hybrid analog–digital beamforming," *IEEE Trans. Wireless Commun*., vol. 15, no. 5, pp. 3311–3326, May 2016.

[18] A. F. Molisch et al., "Hybrid beamforming for massive MIMO: A survey," *IEEE Commun. Mag*., vol. 55, no. 9, pp. 134–141, Sep. 2017.

[19] D. W. Kang, J. G. Kim, B. Min, and G. M. Rebeiz, "Single and fourelement –band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microwave Theory Tech*., vol. 57, no. 12, pp. 3534–3543, Dec. 2009.

[20] A. Valdes-Garcia, S. T. Nicolson, J.-W. Lai, A. Natarajan, P.-Y. Chen, S. K. Reynolds, J.-H. C. Zhan, D. G. Kam, D. Liu, and B. Floyd, "A fully integrated 16-element phased-array transmitter in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2757–2773, 2010

[21] A. Natarajan *et al.*, "A fully-integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1059-1075, May 2011.

[22] Y. Yu, W. Hong, Z. H. Jiang, H. Zhang, and C. Guo, "Multibeam generation and measurement of a DDS-based digital beamforming array transmitter at Ka-band," *IEEE Trans. Antennas Propag*., vol. 67, no. 5, pp. 3020–3039, May 2019.

[23] J. Jeong, N. Collins, and M. P. Flynn, "A 260 MHz IF sampling bit-stream processing digital beamformer with an integrated array of continuous-time band-pass delta-sigma modulators," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1168–1175, May 2016.

[24] H. Aliakbarian, V. Volski, E. van der Westhuizen, R. Wolhuter, and G. A. E. Vandenbosch, "Analogue versus digital for baseband beam steerable array used for LEO satellite applications," *in Proc. 4th Eur. Conf. Antennas Propag. (EuCAP),* 2010, pp. 1–4.

[25] J. Liu, Z. Luo, and X. Xiong, ''Low-resolution ADCs for wireless communication: A comprehensive survey,'' *IEEE Access*, vol. 7, pp. 91291–91324, 2019.

[26] M. Sarajalic, L. Liu, and O. Edfors, "When are low resolution ADCs energy efficient in massive MIMO?" *IEEE Access*, vol. 5, pp. 14837–14853, Nov. 2017

[27] X. Jia, M. Zhou, M. Xie, L. Yang, and H. Zhu, "Optimal design of secrecy massive MIMO amplify-and-forward relaying systems with double-resolution ADCs antenna array," *IEEE Access*, vol. 4, pp. 8757–8774, 2016.

[28] J. Choi, J. Mo, and R. W. Heath, Jr., "Near maximum-likelihood detector and channel estimator for uplink multiuser massive MIMO systems with one-bit ADCs," *IEEE Trans. Commun*., vol. 64, no. 5, pp. 2005–2018, May 2016.

[29] C. Doan, S. Emami, D. Sobel, A. Niknejad, and R. Brodersen, ''Design considerations for 60 GHz CMOS radios,'' *IEEE Commun. Mag*., vol. 42, no. 12, pp. 132–140, Dec. 2004.

[30] T. Nishio, H.-P. Tsai, Y. Wang, and T. Itoh, "A high-speed adaptive antenna array with simultaneous multibeam-forming capability," *IEEE Trans. Microw. Theory Techn*., vol. 51, no. 12, pp. 2483–2494, Dec. 2003.

[31] M. Jahn, R. Feger, C. Wagner, Z. Tong, and A. Stelzer, "A four-channel 94-GHz SiGe-Based digital beamforming FMCW radar," *IEEE Trans. Microw. Theory Techn*., vol. 60, no. 3, pp. 861–869, Mar. 2012.

[32] Y. Zhang *et al*., "DDS-PLL Phased Source for Ka-Band Beam Control Phased Array Receiver," *2018 IEEE Int. Symp. On Antenna, Propagation and EM Theo*ry, Dec. 2018.

[33] Y. Yu, W. Hong, Z. H. Jiang, H. Zhang, and C. Guo, ''Multibeam generation and measurement of a DDS-based digital beamforming array transmitter at Ka-band,'' *IEEE Trans. Antennas Propag.*, vol. 67, no. 5, pp. 3030–3039, May 2019.

[34] K. Gentile and R. Cushing, "A technical tutorial on digital signal synthesis," Analog Devices Inc. 1999, pp. 1–122. [Online]. Available: http://www.analog.com/en/education/education-library/technicaltutorial-dds.html

[35] A. A. Nasir, S. Durrani, H. Mehrpouyan, S. D. Blostein, and R. A. Kennedy, ''Timing and carrier synchronization in wireless communication systems: A survey and classification of research in the last 5 years,'' *EURASIP J. Wirel. Commun. Netw.,* vol. 2016, no. 1, p. 180, 2016.

[36] S. B. Venkatakrishnan et al., "Challenges in Clock Synchronization for On-Site Coding Digital Beamforming", *International Journal of Reconfigurable Computing*, vol. 2017, article ID 7802735, 2017.

[37] S. B. Venkatakrishnan, D. K. Papantonis, A. A. Akhiyat, E. A. Alwan, and J. L. Volakis, "Experimental validation of on-site coding digital beamformer with ultra-wideband antenna arrays," *IEEE Trans. Microw. Theory Techn.,* doi: 10.1109/TMTT.2017.2690451.

[38] P.Poshala and P. Shetty, "Synchronizing the Giga-Sample ADCs Interfaced With Multiple FPGAs," *Application Report SLAA643*, Texas Instruments, Dallas Tex, USA, 2014.

[39] A. Oz and K. Peker, "Synchronizing sample clocks of a data converter array," Analog Devices, Inc., Tech. Rep. Available: https://www.analog.com/en/technical-articles/synchronizing-sample-clocks-of-a-data-converter-array.html

[40] D. Cai, H. Fu, J. Ren, W. Li, N. Li, H. Yu, and K. S. Yeo, "A dividerless PLL with low power and low reference spur by aperture-phase detector and phase-to-analog converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 37–50, Jan. 2013.

[41] A. Li, Y. Chao, X. Chen, L. Wu, and H. C. Luong, "A spur-and-phasenoise-filtering technique for inductor-less fractional-N injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2128–2140, Aug. 2017.

[42] G. V. Tsoulos and M. A. Beach, "Calibration and linearity issues for an

adaptive antenna system," *in Proc. VTC*, vol. 3, May 1997, pp. 1597–1600.
[43] W.-L. Chen, S.-F. Chang, K.-M. Chen, G.-W. Huang, and J.-C. Chang, "Temperature effect on Ku-band current-reused common-gate LNA in 0.13-μm CMOS technology," *IEEE Trans. Microw. Theory Tech*., vol. 57, no. 9, pp. 2131–2138, Sep. 2009.
[44] L. Xie et al., "Hybrid analog-digital antenna array with built-in image injection calibration," *IEEE Trans. Antennas Propag*., vol. 62, no. 11, pp. 5513–5523, Nov. 2014.
[45] L. Wu, H. F. Leung, and A. Li, "A 4-element 60-GHz CMOS phased array receiver with beamforming calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 642–652, Mar. 2017.
[46] B. Sadhu et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.
[47] M. K. Hedayati, A. Abdipour, R. S. Shirazi, C. Cetintepe, and R. B. Staszewski, "A 33-GHz LNA for 5G Wireless Systems in 28-nm Bulk CMOS," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 10, pp. 1460–1464, 2018.
[48] S. Ek et al., "A 28-nm FD-SOI 115-fs Jitter PLL-based LO system for 24-30- GHz sliding-IF 5G transceivers," *IEEE JSSC*, vol. 53, no. 7, pp. 1988-2000, July 2018.
[49] M.-Y. Huang, T. Chi, S. Li, T.-Y. Huang, and H. Wang, "A 24.5– 43.5-GHz ultra-compact CMOS receiver front end with calibrationfree instantaneous full-band image rejection for multiband 5G massive MIMO," *IEEE J. Solid-State Circuit*s, vol. 55, no. 5, pp. 1177–1186, May 2020
[50] J. Pang et al., "A 28 GHz CMOS phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized MIMO for 5G NR," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 344–346.
[51] Y. Wang et al., "A 39-GHz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5G NR in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1249–1269, May 2020.
[52] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz linear Doherty power amplifier in silicon for 5G applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, Jun. 2019.
[53] S. Ahmadi Mehr, M. Tohidian, and R. Staszewski, "Toward solving multichannel RF-SoC integration issues through digital fractional division," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*., vol. 24, no. 3, pp. 1071–1082, Mar. 2016.

Dong-Chan Kim received the B.S. degree in Electronic and Electrical Engineering from Sungkyunkwan University,W Suwon, Korea, in 2015, and the M.S. degree in School of Electrical Engineering in school of Electrical Engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2017, where he is currently working toward the Ph.D. degree.
His current research interests are design of frequency modulated continuous wave radar systems, radar signal processing, and digital beamforming.

Ye-Eun Chi received the B.S. degree in electronic engineering from Ewha Womans University, Seoul, South Korea, in 2016, and the M.S. degree from the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2019, where she is currently pursuing the Ph.D. degree.
Hers current research interests include the design of millimeter-wave system, self-calibration system, and MIMO beamforming.

Junhyeong Park (GS'18) received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2017. He is currently pursuing the Ph.D. degree in electrical engineering at KAIST.
His current research interests include radar systems for defense, drone detection radar, radar imaging, target recognition/classification, and radar signal processing.

Laxmikant Minz born in Katihar, India in September 1986. He received the B.Tech degree in electronic and communication engineering from NIT Nagpur, India, in 2007 and M.Tech degree in RF and Microwave engineering from IIT Kharagpur, India, in 2009. He worked as researcher with antenna development team in ETRI, Daejeon (SouthKorea) for 5 years. Currently, he is working toward the Ph.D. degree in School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST).
His research interests focused on antenna and array design, microstrip miniaturized antenna, Radar system, metamaterial, electromagnetics and microwave circuit design.

Seong-Ook Park (M'05-SM'11) received the B.S. degree from KyungPook National University, Korea, in 1987, the M.S. degree from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 1989, and the Ph.D. degree from Arizona State University, Tempe, in 1997, all in electrical engineering. From March 1989 to August 1993, he was a Research Engineer with Korea Telecom, Daejeon, working with microwave systems and networks. He later joined the Telecommunication Research Center, Arizona State University, until September 1997.
Since October 1997, he has been a Professor at the Korea Advanced Institute of Science and Technology. His research interests include antenna, radar system, and analytical and numerical techniques in the area of electromagnetics.